

WT01P461-S1 Datasheet



Version 1.1

Disclaimer and Copyright Notice

Information in this document, including the URL addresses for reference, is subject to change without notice.

This document is provided "as is" without warranty of any kind, including any warranty of merchantability, fitness for a particular purpose, or non-infringement, and any warranty that any proposal, specification, or sample is referred to elsewhere. This document disclaims all liability, including liability for infringement of any patent, arising out of the use of the information in this document. This document does not grant any license, express or implied, by estoppel or otherwise, to use any intellectual property.

The Wi-Fi Alliance member logo is owned by the Wi-Fi Alliance.

All trade names, trademarks and registered trademarks mentioned herein are the property of their respective owners and are hereby acknowledged.

Notice

The content of this manual is subject to change due to product version upgrade or other reasons. WIRELESS-TAG Technology Co.,limited reserves the right to modify the contents of this manual without any notice or prompting. Ltd. makes every effort to provide accurate information in this manual, but WIRELESS-TAG Technology Co.,limited does not ensure that the contents of the manual are completely free of errors, and all statements, information and recommendations in this manual do not constitute any express or implied warranty.



Revision History

Version	Date	Developed/ Changed Content	Modifier By	Auditor
V1.0	2026-3-25	First Creation	Pail	Louie
V1.1	2026-6-25	1.Modified 1.1. Part Number in the Products Introduction 2.Updated 1.3. Product Pictures Content 3.Corrected an error in 3.4. Other Pin Descriptions	Pail	Louie



Contents

1. Overview	5
1.1. Products Introduction	5
1.2. Product Features	6
1.3. Product Pictures	6
1.4. Application Scenarios	6
2. Product Specification	7
2.1. Block Diagram	7
2.2. Hardware Parameters	8
3. Pin Definitions	10
3.1. Pin Layout	10
3.2. Pin Description	10
3.3. Startup Item Configuration	14
3.3.1. ESP32-P4 Strapping Pins	14
3.3.2. ESP32-P4 Chip Boot Mode Control	15
3.3.3. ESP32-P4 ROM Messages Printing Control	15
3.3.4. ESP32-C61 Strapping Pins	16
3.3.5. ESP32-C61 Chip Boot Mode Control	18
3.3.6. ESP32-C61 ROM Messages Printing Control	19
3.3.7. ESP32-C61 JTAG Signal Source Control	19
3.4. Other Pin Descriptions	20
4. Electrical Characteristics	21
4.1. Absolute Maximum Limit Value	21
4.2. Power Consumption Characteristics	21
4.3. Recommended Working Conditions	21
5. WT01P461-S1 Schematic	21
6. WT01P461-S1 Dimensions	22
7. Storage Condition	22
8. Reflow Soldering Curve	23
9. Contact Us	23

1. Overview

1.1. Products Introduction

WT01P461-S1, a core board with integrated 2.4GHz Wi-Fi6 and NOR FLASH based on Espressif's ESP32-P4 and ESP32-C61 series chips designed by Wireless-Tag Technology Co., Limited. The core processor chip, ESP32-P4, is stackable with either 16MB or 32MB PSRAM in a package that includes a high-performance (HP) system and a low-power (LP) system. The HP system is a RISC-V dual-core processor running at 400MHz and includes a JPEG codec, Pixel-Processing Accelerator, H.264 video encoder, and MIPI interfaces, providing powerful image and voice processing capabilities. The ESP32-C61 high-performance SOC on the core board supports 2.4 Wi-Fi6 (802.11ax) and Bluetooth®5 (LE). The ESP32-P4 and ESP32-C61 on the core board are connected via their SDIO interface, and the rest of the pins are already pinned out.

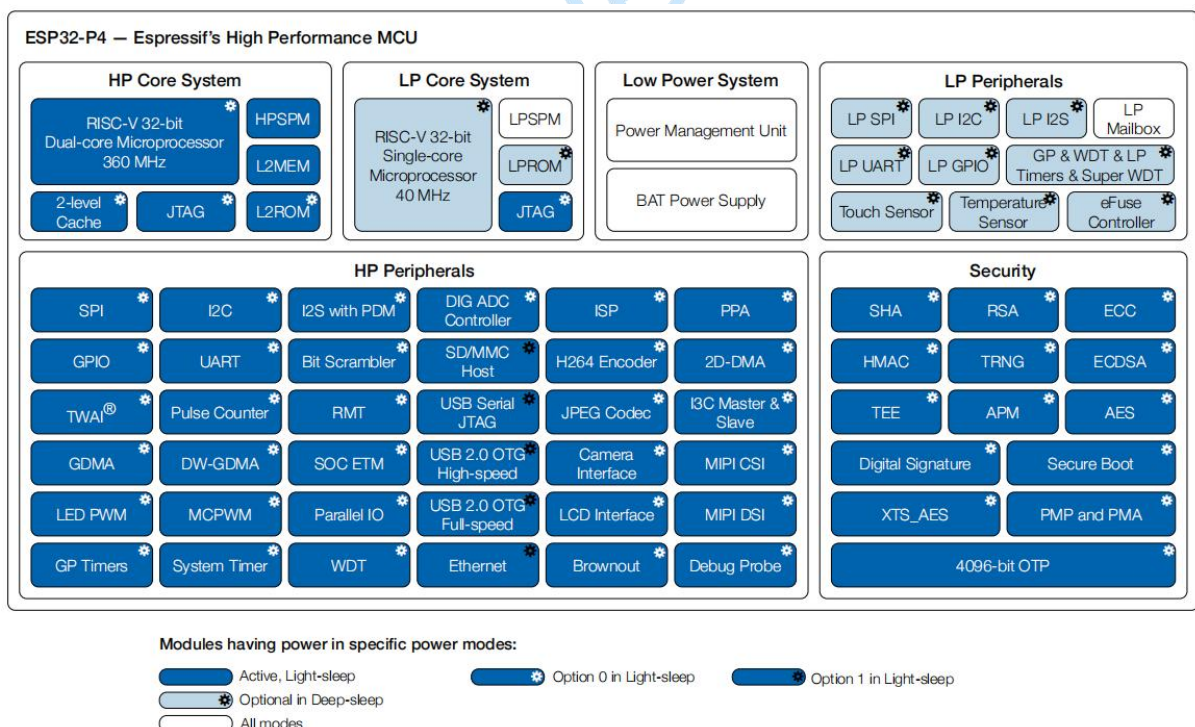


Figure 1: Main Chip Architecture Diagram

The WT01P461-S1 series is available in two sizes, see the table below for more information.

WT01P461-S1 Series Model Number Comparison

Part Number	Flash	Psram	Module Size (mm)
WT01P461-S1-N16R16X	16MB	16MB	25.00*25.00
WT01P461-S1-N16R32X	16MB	32MB	25.00*25.00

1.2.Product Features

- Dual-core 400 MHz high-frequency CPU
- 16 MB Flash and 16/32 MB Psram
- supports 2.4GHz Wi-Fi6, BLE5
- ESP32-P4 and ESP32-C61 chip with full pinout
- Supports multiple multimedia interfaces
- Core board size is small, easy to hardware design
- Development materials are complete

1.3.Product Pictures



Figure 2:WT01P461-S1(front)



Figure 3:WT01P461-S1 (back)



Figure 4:WT01P461-S1(front)



Figure 5:WT01P461-S1(back)

1.4.Application Scenarios

- Smart Home
- Industrial Automation
- Consumer Electronics
- HMI Human Machine Interaction

- Electronic Robotics
- Camera Video Streaming
- USB Devices
- Healthcare

2. Product Specification

2.1. Block Diagram

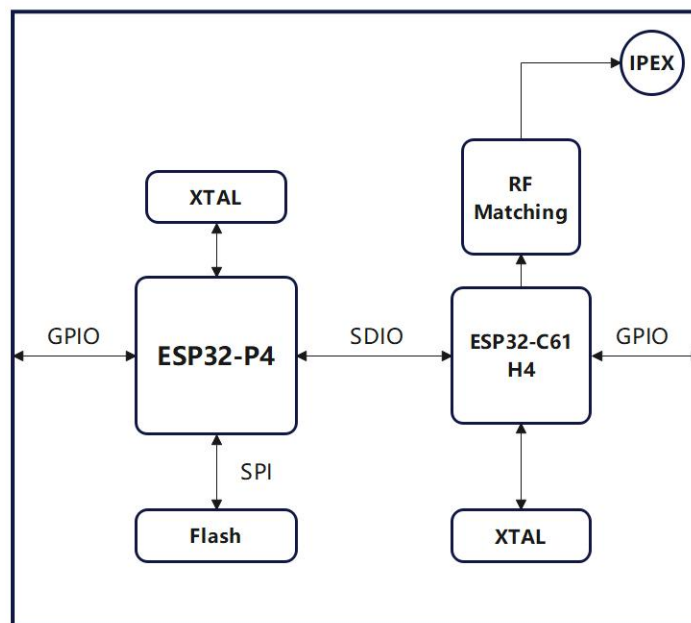


Figure 6: Block diagram of WT01P461-S1

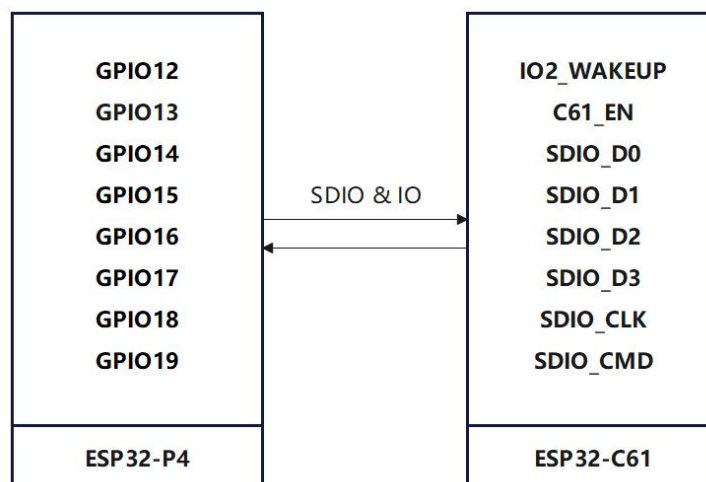


Figure 7: P4 & C61 Pin Correspondence Diagram

2.2. Hardware Parameters

ESP32-P4	Core	32-bit RISC-V dual-core
	Main Frequency	400 MHz (HP Core)
		40 MHz (LP Core)
ESP32-C61	Core	32-bit RISC-V single-core
	Main Frequency	160 MHz
Memory	ESP32-P4 ROM	128 KB HP ROM
		16 KB LP ROM
	ESP32-P4 SRAM	768 KB HP L2MEM
		32 KB LP SRAM
	ESP32-P4 PSRAM	16/32 MB
	ESP32-C61 ROM	256 KB
	ESP32-C61 SRAM	320 KB
	P4 Flash	16 MB
	C61 Flash	4 MB
ESP32-P4 Peripheral Interface	GPIO	46
	SPI	2
	LP SPI	1
	UART	5
	LP UART	1
	I3C	1
	I2C	2
	LP I2C	1
	I2S	3
	LP I2S	1
	USB JTAG	1
	LED PWM	1
	MCPWM	2

	TWAI®Controller (compatible with ISO 11898-1)	3
	Hight-Speed USB 2.0 OTG	1
	Full-Speed USB 2.0 OTG	1
	100 Mbit Ethernet	1
	MIPI CSI-2	1
	MIPI DSI	1
	Parallel IO interface	1
	12-bit multi-channel ADC	2
	Temperature sensor	1
	Touch sensor	1
	Analog voltage comparator	1
	Brown-out detector	1
ESP32-C61 Peripheral Interface	GPIO	8
	SPI	1
	UART	3
	I2C	1
	I2S	1
	LED PWM	1
	12-bit multi-channel ADC	1
	Temperature sensor	1
Image and Voice Processing Functionality	JPEG Codec	1
	PPA	1
	ISP	1
	H264 encoder	1

3. Pin Definitions

3.1.Pin Layout

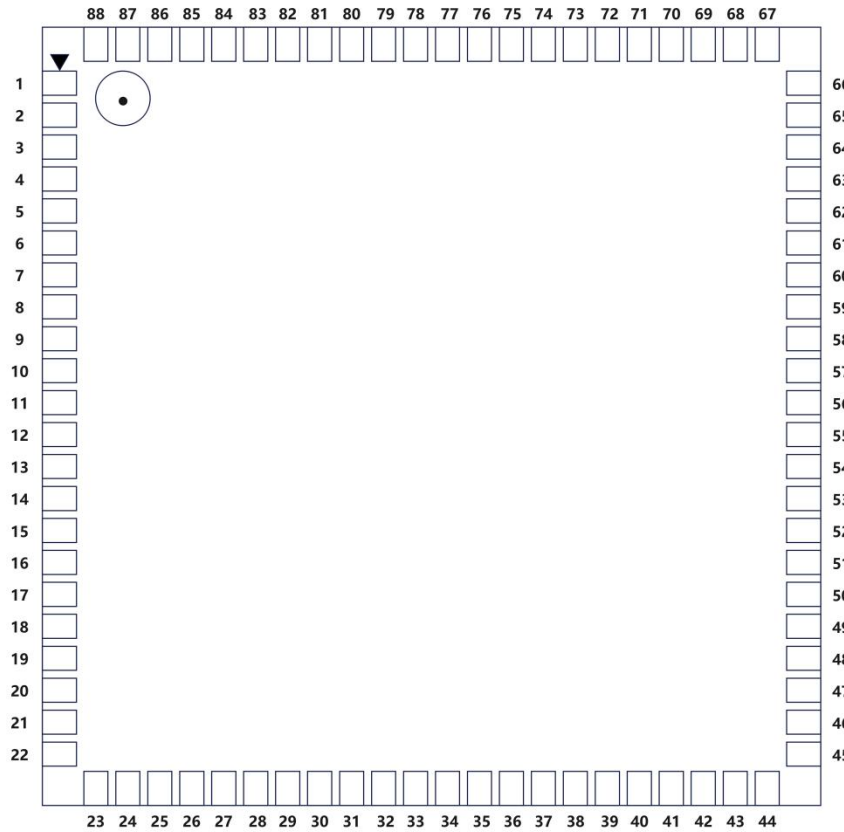


Figure 8:WT01P461-S1 Pin Layout

3.2.Pin Description

Pin Definitions

No.	Name	Function
1	GND	GROUND
2	ANT	2.4G Antenna pin
3	GND	GROUND
4	C61_U0RXD	GPIO10, U0RXD
5	C61_U0TXD	GPIO11, U0TXD
6	C61_EN	Enable ESP32-C61 (internal 10K pull-up)
7	C61_GPIO0	GPIO0, LP_GPIO0, XTAL_32K_P
8	C61_GPIO1	GPIO1, LP_GPIO1, XTAL_32K_N, ADC1_CHO
9	C61_GPIO4	GPIO4, LP_GPIO4, MTDI, ADC1_CH2, FSPIWP

10	C61_GPIO5	GPIO5, LP_GPIO5, MTCK, ADC1_CH3
11	C61_GPIO6	GPIO6, LP_GPIO6, MTDO, FSPICLK
12	C61_GPIO7	GPIO7, FSPID
13	C61_GPIO8	GPIO8, FSPICS0, ZCD0 (internal 10K pull-up)
14	C61_GPIO9	GPIO9, ZCD1 (internal 10K pull-up)
15	GND	GROUND
16	GPIO1	GPIO1, LP_GPIO1, XTAL_32K_P
17	GPIO2	GPIO2, MTCK, LP_GPIO2, TOUCH_CHANNEL1
18	GPIO3	GPIO3, MTDI, LP_GPIO3, TOUCH_CHANNEL2
19	GPIO4	GPIO4, MTMS, LP_GPIO4, TOUCH_CHANNEL3
20	GPIO5	GPIO5, MTDO, LP_GPIO5, TOUCH_CHANNEL4
21	GPIO6	GPIO6, SPI2_HOLD_PAD, LP_GPIO6, TOUCH_CHANNEL5
22	GPIO7	GPIO7, SPI2_CS_PAD, LP_GPIO7, TOUCH_CHANNEL6
23	GPIO8	GPIO8, UART0_RTS_PAD, SPI2_D_PAD, LP_GPIO8, TOUCH_CHANNEL7
24	GPIO9	GPIO9, UART0_CTS_PAD, SPI2_CK_PAD, LP_GPIO9, TOUCH_CHANNEL8
25	GPIO10	GPIO10, UART1_TXD_PAD, SPI2_Q_PAD, LP_GPIO10, TOUCH_CHANNEL9
26	GPIO11	GPIO11, UART1_RXD_PAD, SPI2_WP_PAD, LP_GPIO11, TOUCH_CHANNEL10
27	GPIO20	GPIO20, ADC1_CHANNEL4
28	GPIO21	GPIO21, ADC1_CHANNEL5
29	GPIO22	GPIO22, ADC1_CHANNEL6
30	GPIO23	GPIO23, ADC1_CHANNEL7, REF_50M_CLK_PAD
31	GND	GROUND
32	DSI_DATAP1	MIPI DSI PHY DATAP1
33	DSI_DATAN1	MIPI DSI PHY DATAN1

34	DSI_CLKN	MIPI DSI PHY CLKN
35	DSI_CLKP	MIPI DSI PHY CLKP
36	DSI_DATAP0	MIPI DSI PHY DATAP0
37	DSI_DATAN0	MIPI DSI PHY DATAN0
38	GND	GROUND
39	CSI_DATAN0	MIPI CSI PHY DATAN0
40	CSI_DATAP0	MIPI CSI PHY DATAP0
41	CSI_CLKP	MIPI CSI PHY CLKP
42	CSI_CLKN	MIPI CSI PHY CLKN
43	CSI_DATAN1	MIPI CSI PHY DATAN1
44	CSI_DATAP1	MIPI CSI PHY DATAP1
45	GND	GROUND
46	USB_DM	USB2 OTG PHY DM
47	USB_DP	USB2 OTG PHY DP
48	GPIO24	GPIO24, USB1P1_N0
49	GPIO25	GPIO25, USB1P1_P0
50	GND	GROUND
51	GPIO26	GPIO26, USB1P1_N1
52	GPIO27	GPIO27, USB1P1_P1
53	GPIO28	GPIO28, SPI2_CS_PAD, GMAC_PHY_RXDV_PAD
54	GPIO29	GPIO29, SPI2_D_PAD, GMAC_PHY_RXD0_PAD
55	GPIO30	GPIO30, SPI2_CK_PAD, GMAC_PHY_RXD1_PAD
56	GPIO31	GPIO31, SPI2_Q_PAD, GMAC_PHY_RXER_PAD
57	GPIO32	GPIO32, SPI2_HOLD_PAD, GMAC_RMII_CLK_PAD
58	GPIO33	GPIO33, SPI2_WP_PAD, GMAC_PHY_TXEN_PAD
59	GPIO34	GPIO34, SPI2_IO4_PAD, GMAC_PHY_TXD0_PAD
60	GPIO35	GPIO35, SPI2_IO5_PAD, GMAC_PHY_TXD1_PAD (internal 10K pull-up)
61	GPIO36	GPIO36, SPI2_IO6_PAD, GMAC_PHY_TXER_PAD (internal 10K pull-up)

62	GPIO37	GPIO37, UART0_TXD_PAD, SPI2_IO7_PAD (ESP32-P4 Download Pin)
63	GPIO38	GPIO38, UART0_RXD_PAD, SPI2_DQS_PAD (ESP32-P4 Download Pin)
64	ESP_LDO_VO4	Output POWER (Output voltage range 0.5~2.7V or 3.3V, maximum output current 0.2A)
65	GND	GROUND
66	GPIO39	GPIO39, SD1_CDATA0_PAD, REF_50M_CLK_PAD
67	GPIO40	GPIO40, SD1_CDATA1_PAD, GMAC_PHY_TXEN_PAD
68	GPIO41	GPIO41, SD1_CDATA2_PAD, GMAC_PHY_TXD0_PAD
69	GPIO42	GPIO42, SD1_CDATA3_PAD, GMAC_PHY_TXD1_PAD
70	GPIO43	GPIO43, SD1_CCLK_PAD, GMAC_PHY_TXER_PAD
71	GPIO44	GPIO44, SD1_CCMD_PAD, GMAC_RMII_CLK_PAD
72	GPIO45	GPIO45, SD1_CDATA4_PAD, GMAC_PHY_RXDV_PAD
73	GPIO46	GPIO46, SD1_CDATA5_PAD, GMAC_PHY_RXD0_PAD
74	GPIO47	GPIO47, SD1_CDATA6_PAD, GMAC_PHY_RXD1_PAD
75	GPIO48	GPIO48, SD1_CDATA7_PAD, GMAC_PHY_RXER_PAD
76	GPIO49	GPIO49, GMAC_PHY_TXEN_PAD, ADC2_CHANNEL0
77	GPIO50	GPIO50, GMAC_RMII_CLK_PAD, ADC2_CHANNEL1
78	GPIO51	GPIO51, GMAC_PHY_RXDV_PAD, ADC2_CHANNEL2, ANA_COMP0
79	GPIO52	GPIO52, GMAC_PHY_RXD0_PAD, ADC2_CHANNEL3, ANA_COMP0
80	GPIO53	GPIO53, GMAC_PHY_RXD1_PAD, ADC2_CHANNEL4, ANA_COMP1
81	GPIO54	GPIO54, GMAC_PHY_RXER_PAD, ADC2_CHANNEL5, ANA_COMP1
82	GND	GROUND
83	GND	GROUND
84	VBAT	battery power supply pin
85	ESP_3V3	POWER (3.3V input for core board power supply)
86	ESP_3V3	POWER (3.3V input for core board power supply)

87	P4_EN	Enable ESP32-P4 (internal 10K pull-up)
88	GPIO0	GPIO0, LP_GPIO0, XTAL_32K_N

3.3.Startup Item Configuration

3.3.1. ESP32-P4 Strapping Pins

The chip allows for configuring the following boot parameters through strapping pins and eFuse bits at power-up or a hardware reset, without microcontroller interaction.

- **Chip Boot Mode**

- Strapping pin: GPIO35, GPIO36, GPIO37 and GPIO38

- **ROM Message Printing**

- Strapping pin: GPIO36

- eFuse bit: EFUSE_UART_PRINT_CONTROL

- **JTAG Signal Source**

- Strapping pin: GPIO34

- eFuse bit: EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG and EFUSE_JTAG_SEL_ENABLE

The default values of all the above eFuse bits are 0, which means that they are not burnt. Given that eFuse is one-time programmable, once an eFuse bit is programmed to 1, it can never be reverted to 0.

The default values of the strapping pins, namely the logic levels, are determined by pins' internal weak pull-up/pull-down resistors at reset if the pins are not connected to any circuit, or connected to an external high-impedance circuit.

Default Configuration of Strapping Pin

Strapping Pin	Default Configuration	Value
GPIO34	Floating	-
GPIO35	Weak pull-up	1
GPIO36	Floating	-

GPIO37	Floating	-
GPIO38	Floating	-

To change the bit values, the strapping pins should be connected to external pull-down/pull-up resistors. If the ESP32-P4 is used as a device by a host MCU, the strapping pin voltage levels can also be controlled by the host MCU.

All strapping pins have latches. At system reset, the latches sample the bit values of their respective strapping pins and store them until the chip is powered down or shut down. The states of latches cannot be changed in any other way. It makes the strapping pin values available during the entire chip operation, and the pins are freed up to be used as regular IO pins after reset.

3.3.2. ESP32-P4 Chip Boot Mode Control

GPIO35 ~ GPIO38 control the boot mode after the reset is released.

Boot Mode	GPIO35	GPIO36	GPIO37	GPIO38
SPI Boot*	1*	Any value	Any value	Any value
Joint Download Boot	0	1	Any value	Any value

*marks the default value and configuration.

Joint Download Boot mode supports the following download methods:

- USB Download Boot:
 - USB-Serial-JTAG Download Boot
 - USB 2.0 OTG Download Boot
- UART Download Boot
- SPI Slave Download Boot

3.3.3. ESP32-P4 ROM Messages Printing Control

During the boot process, the messages by the ROM code can be printed to:

- **(Default) UART0 and USB Serial/JTAG controller**
- USB Serial/JTAG controller
- UART0

EFUSE_UART_PRINT_CONTROL and GPIO36 control ROM messages printing to UART0 as shown in Table.

UART0 Code Printing	EFUSE_UART_PRINT_CONTROL	GPIO36
Enabled*	0*	Ignored
	1	0
	2	1
Disabled	1	1
	2	0
	3	Ignored

*marks the default value and configuration.

EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT controls the printing to USB Serial/JTAG controller as shown in Table.

USB Serial/JTAG ROM Code Printing	EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT
Enabled*	0*
Disabled	1

*marks the default value and configuration.

3.3.4. ESP32-C61 Strapping Pins

The chip allows for configuring the following boot parameters through strapping pins and eFuse bits at power-up or a hardware reset, without microcontroller interaction.

- **Chip Boot Mode**

- Strapping pin: GPIO8 and GPIO9

- **ROM Message Printing**

- Strapping pin: GPIO8

- eFuse parameter:

EFUSE_UART_PRINT_CONTROL and EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT

- **JTAG Signal Source**

- Strapping pin: GPIO7

- eFuse parameter:

EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG, and EFUSE_JTAG_SEL_ENABLE

The default values of all the above eFuse parameters are 0, which means that they are not burnt. Given that eFuse is one-time programmable, once programmed to 1, it can never be reverted to 0.

The default values of the strapping pins, namely the logic levels, are determined by pins' internal weak pull-up/pull-down resistors at reset if the pins are not connected to any circuit, or connected to an external high-impedance circuit.

Default Configuration of Strapping Pin

Strapping Pin	Default Configuration	Value
GPIO7	Floating	-
GPIO8	Floating	-
GPIO9	Pull-up	1

To change the bit values, the strapping pins should be connected to external pull-down/pull-up resistors.

All strapping pins have latches. At system reset, the latches sample the bit values of their respective strapping pins and store them until the chip is powered down or shut down. The states of latches cannot be changed in any other way. It makes the strapping pin values available during the entire chip operation, and the pins are freed up to be used as regular IO pins after reset.

The timing of signals connected to the strapping pins should adhere to the *setup time* and *hold time* specifications in Table and Figure 8.

Description of Timing Parameters for the Strapping Pins

Parameter	Description	Min (ms)
t_{SU}	<i>Setup time</i> is the time reserved for the power rails to stabilize before the CHIP_PU pin is pulled high to activate the chip.	0
t_H	<i>Hold time</i> is the time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as	3

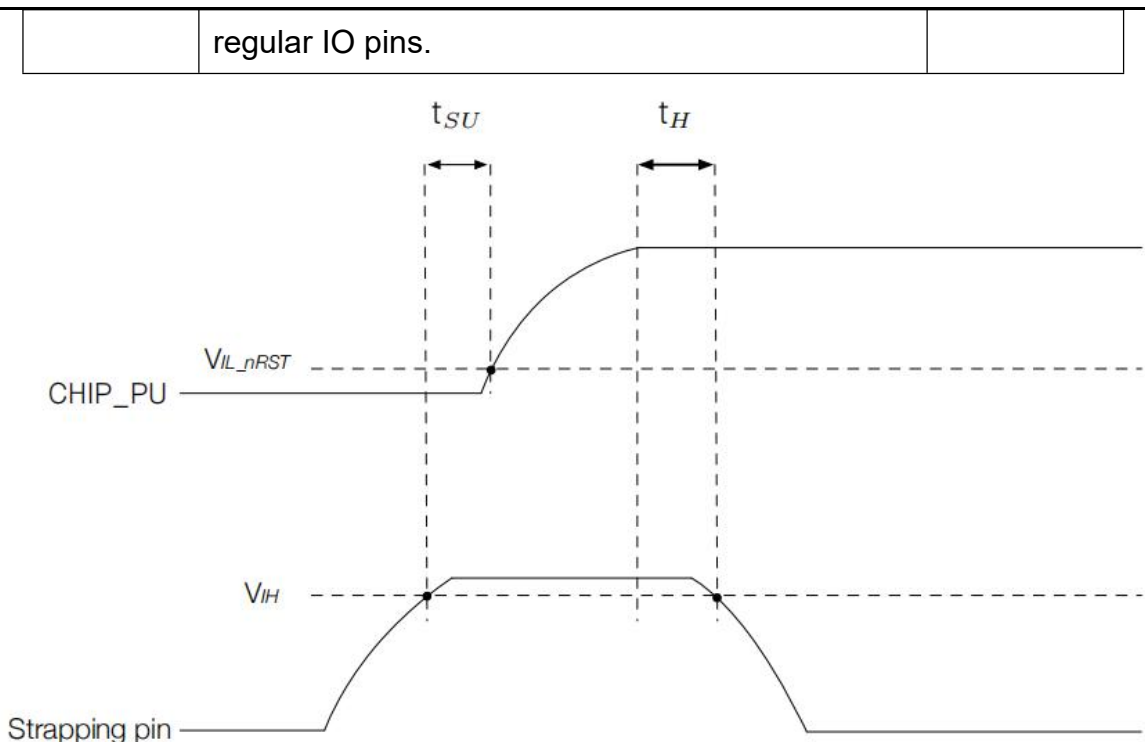


Figure 9: Visualization of Timing Parameters for the Strapping Pins

3.3.5. ESP32-C61 Chip Boot Mode Control

GPIO8 and GPIO9 control the boot mode after the reset is released.

Boot Mode	GPIO8	GPIO9
SPI Boot*	Any value	1
Joint Download Boot ¹	1	0

*marks the default value and configuration.

¹Joint Download Boot mode supports the following download methods:

- USB-Serial-JTAG Download Boot
- UART Download Boot
- SDIO Slave 2.0 Download Boot

In SPI Boot mode, the ROM bootloader loads and executes the program from SPI flash to boot the system.

In Joint Download Boot mode, users can download binary files into flash using UART0, USB or SDIO Slave interfaces and execute it in SPI Boot mode.

In Joint Download Boot mode,, it is also possible to download binary files into SRAM using UART0, USB or SDIO Slave interfaces and execute it from SRAM.

3.3.6. ESP32-C61 ROM Messages Printing Control

During the boot process, the messages by the ROM code can be printed to:

- **(Default) UART0 and USB Serial/JTAG controller**
- USB Serial/JTAG controller
- UART0

EFUSE_UART_PRINT_CONTROL and GPIO8 control ROM messages printing to **UART0** as shown in Table.

UART0 ROM Code Printing	EFUSE_UART_PRINT_CONTROL	GPIO8	Register ¹
Always enabled*	0*	Ignored	0
Enabled	1	0	
Disabled		1	
Disabled	2	0	
Enabled		1	
Always enabled	3	Ignored	
Disabled	Ignored	Ignored	1

*marks the default value and configuration.

¹Register: LP_AON_STORE4_REG[0]

EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT controls the printing to USB Serial/JTAG controller as shown in Table.

USB Serial/JTAG ROM Message Printing Control	LP_AON_STORE4_REG[0]	EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT
Enabled*	0*	0*
Disabled	0	1
	1	Ignored

*marks the default value and configuration.

3.3.7. ESP32-C61 JTAG Signal Source Control

The strapping pin GPIO7 can be used to control the source of JTAG signals during the early boot process. This pin does not have any internal pull resistors

and the strapping value must be controlled by the external circuit that cannot be in a high impedance state.

GPIO7 is used in combination with

EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG, and EFUSE_JTAG_SEL_ENABLE.

JTAG Signal Source	eFuse 1 ¹	eFuse 2 ²	eFuse 3 ³	GPIO7
USB Serial/JTAG Controller ^{*5}	0 [*]	0 [*]	0 [*]	X ⁴
			1	1
JTAG pins MTDI, MTCK, MTMS, and MTDO	0	x	x	0
				x
USB Serial/JTAG Controller	0	1	x	x
USB Serial/JTAG Controller	1	0	x	x
JTAG is disabled	1	1	x	x
	1	x	x	x

*marks the default value and configuration.

¹eFuse 1: EFUSE_DIS_PAD_JTAG

²eFuse 2: EFUSE_DIS_USB_JTAG

³eFuse 3: EFUSE_JTAG_SEL_ENABLE

⁴x: x indicates that the value has no effect on the result and can be ignored

3.4. Other Pin Descriptions

The GPIO12 and GPIO13 pins of the ESP32-P4 chip on the core board are connected to the GPIO2 and CHIP_PU pins of the ESP32-C61 chip on the core board (see table below). The ESP32-P4 can wake up the ESP32-C61 via GPIO12. and the ESP32-P4 can reset the ESP32-C61 via GPIO13.

ESP32-P4	ESP32-C61
GPIO12	GPIO2
GPIO13	CHIP_PU

The ESP32-P4 and ESP32-C61 chips on the core board communicate via the SDIO interface; see the figure below for the pin mapping.

ESP32-P4 Pin Numbers and Descriptions		ESP32-C61 Pin Numbers and Descriptions	
15	GPIO14	15	SDIO_DATA0
16	GPIO15	16	SDIO_DATA1
17	GPIO16	17	SDIO_DATA2
18	GPIO17	18	SDIO_DATA3
19	GPIO18	14	SDIO_CLK
20	GPIO19	13	SDIO_CMD

4. Electrical Characteristics

4.1. Absolute Maximum Limit Value

Exceeding the absolute maximum ratings may result in permanent damage to the device. This is an emphasized rating only and does not address the functional operation of the device under these or other conditions beyond those indicated in these specifications. Prolonged exposure to absolute maximum rating conditions may affect module reliability.

4.2. Power Consumption Characteristics

update soon

4.3. Recommended Working Conditions

Parameter	Description	Min	Typ	Max	Unit
VCC	Power pin voltage	3.0	3.3	3.6	V
I _{VCC}	Supply current from external power supply	-	1	-	A
T _A	Operating Temperature	-40	-	85	°C

5. WT01P461-S1 Schematic

update soon

Figure 10: WT01P461-S1 Schematic

6. WT01P461-S1 Dimensions

The following figure shows the top view and front view of WT01P461-S1 with a tolerance of ± 0.2 mm.

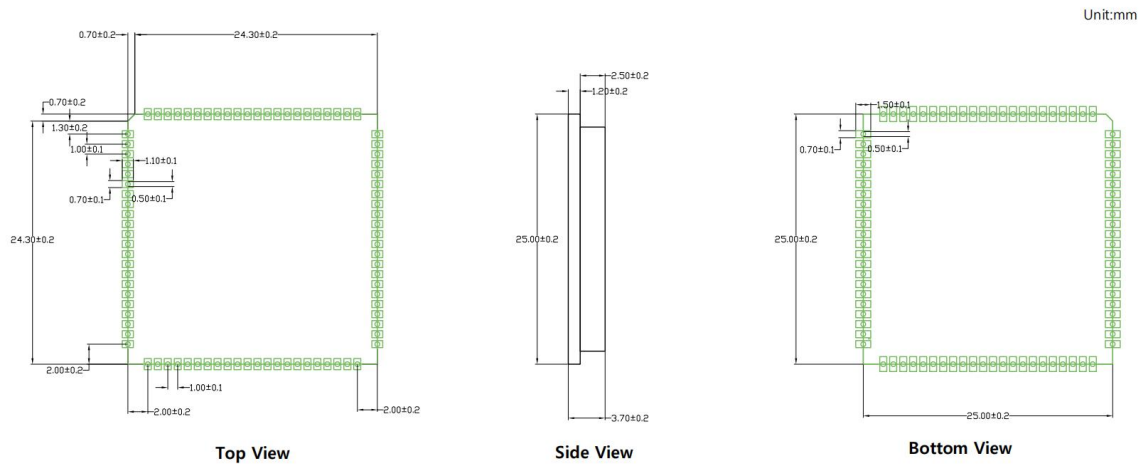


Figure 11: Dimension figure of WT01P461-S1

7. Storage Condition

Prerequisite	Parameters
Storage condition	Non-condensing atmosphere < 40℃ /90 %RH in sealed MBBs
Conditions of use	168 hours at 25 ± 5℃ , 60 % RH.
Moisture sensitivity	3 levels

8. Reflow Soldering Curve

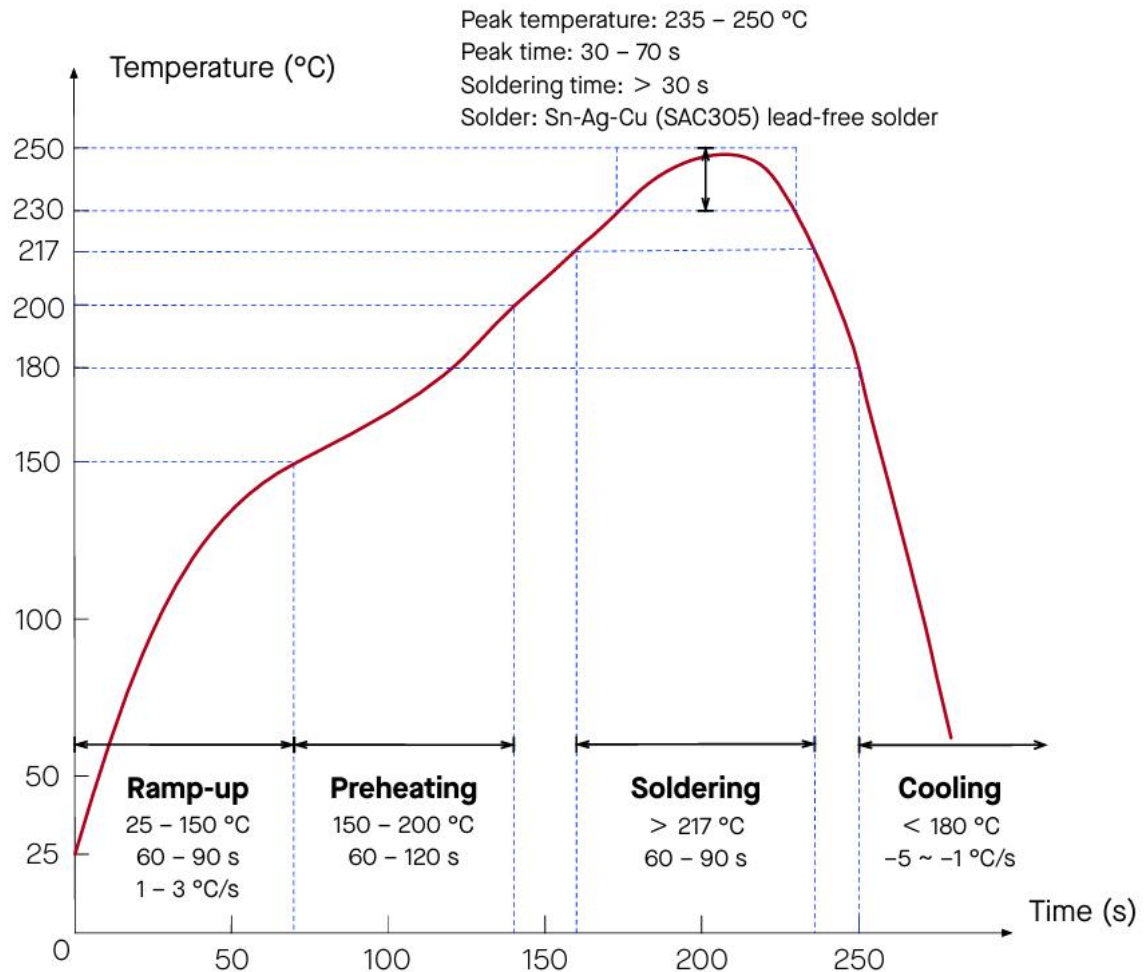


Figure 12: Reflow Soldering Temperature Curve

9. Contact Us

Official website: www.wireless-tag.com

Contact Email: gtm@wireless-tag.com

Technical support e-mail: technical@wireless-tag.com